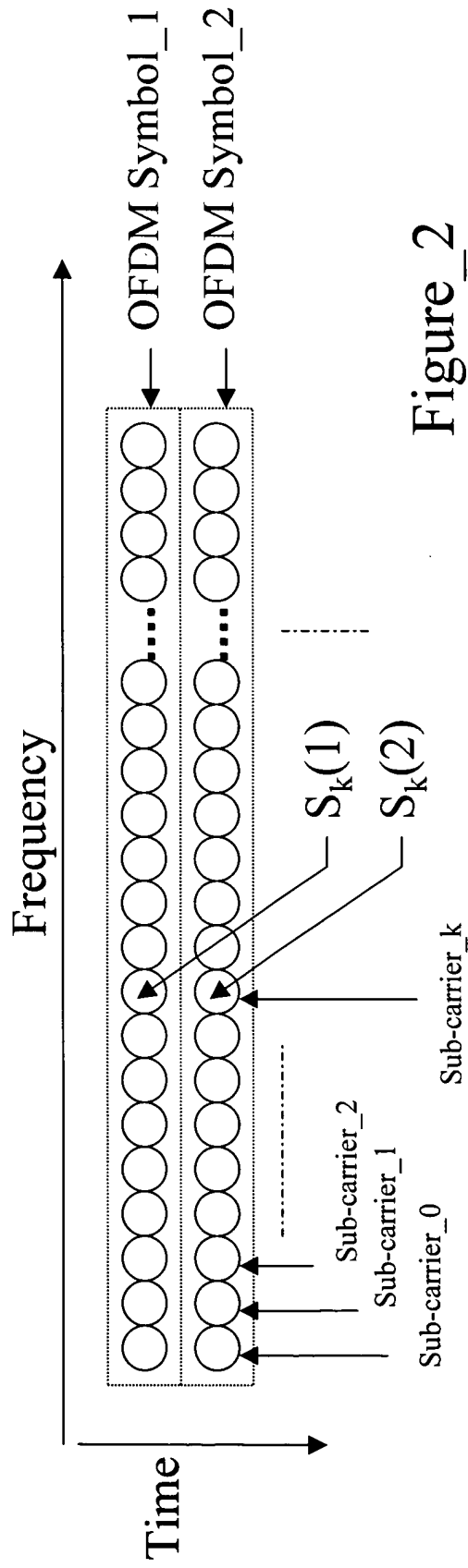
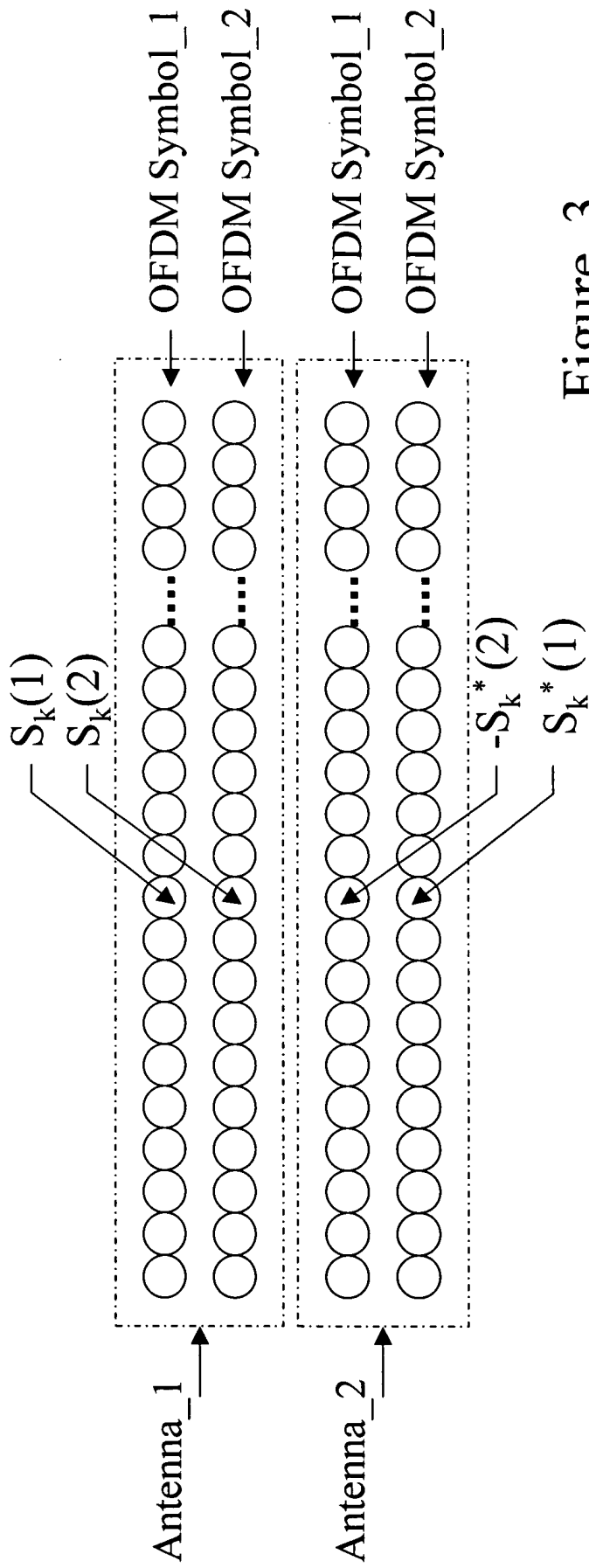


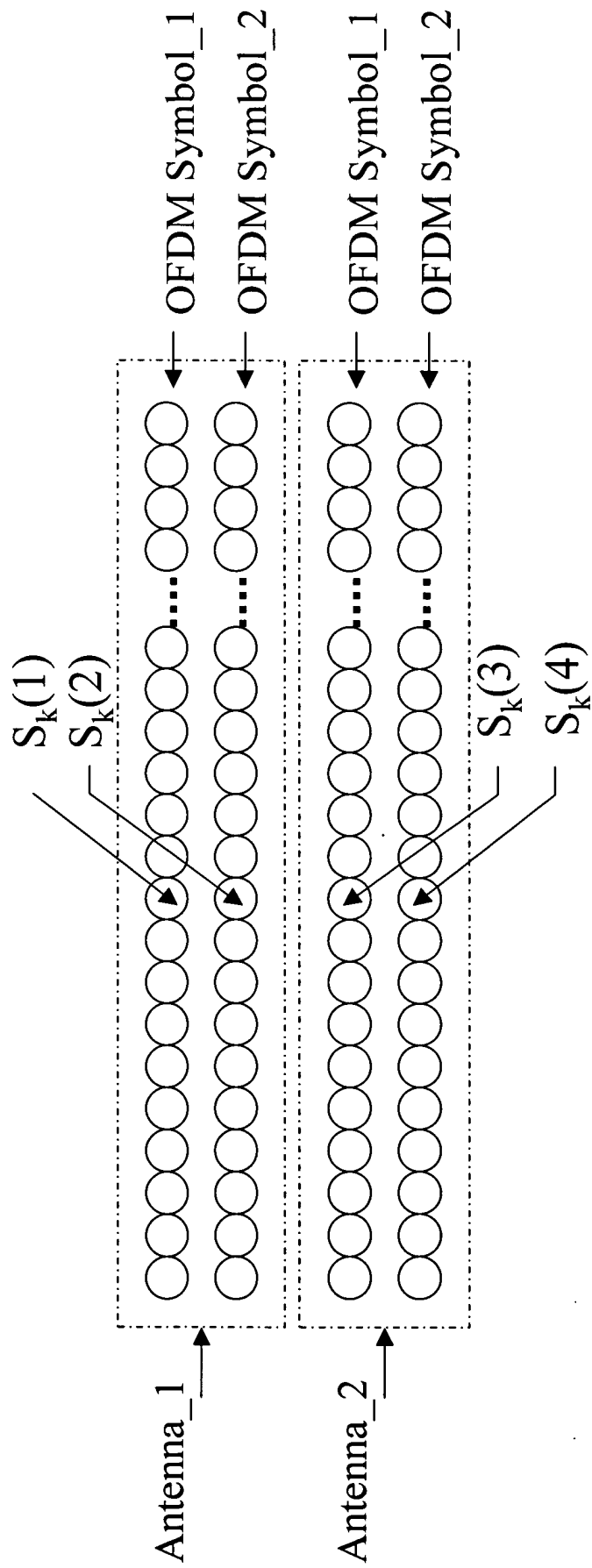
**Figure-1**



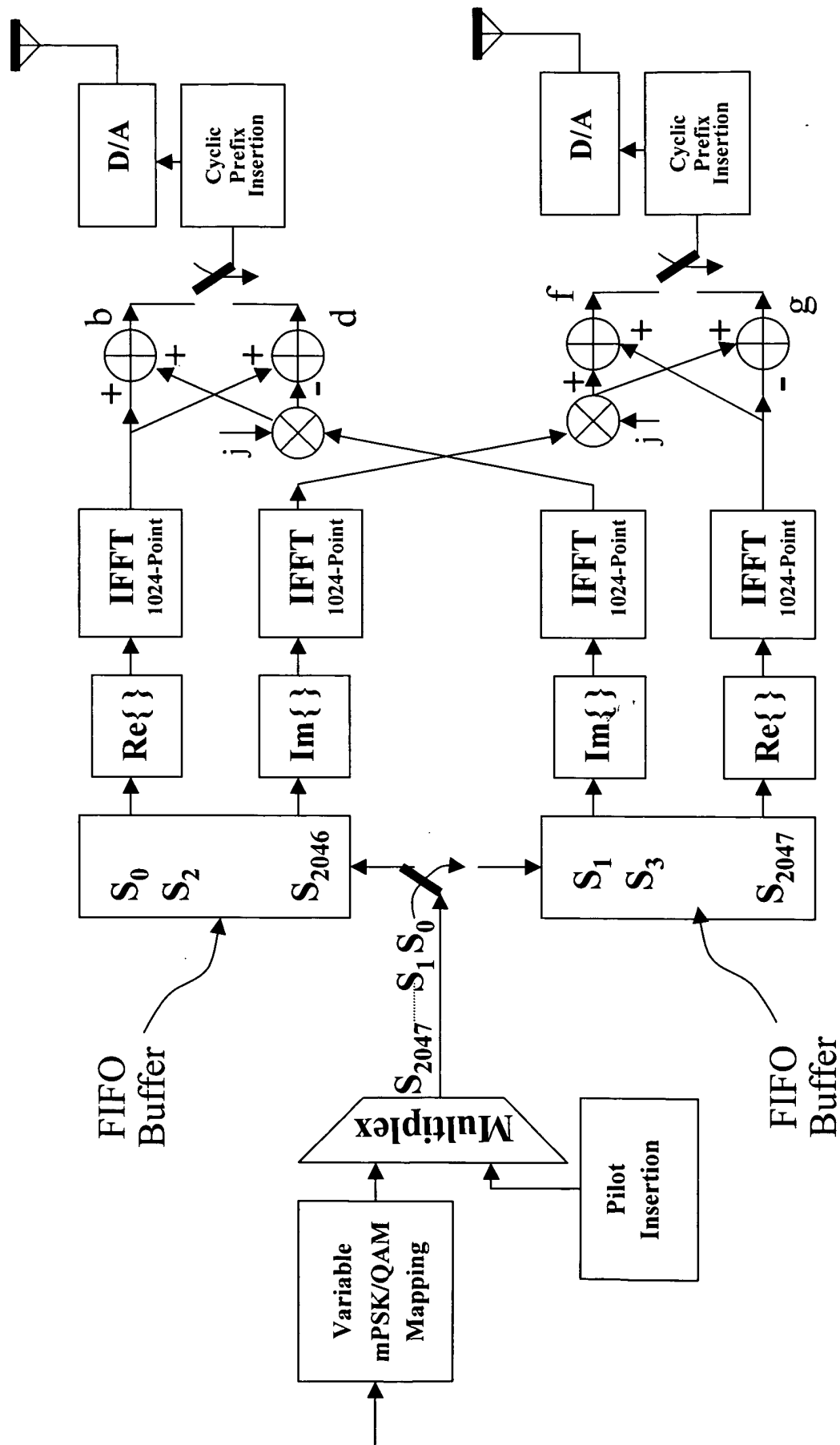
Figure\_2



Figure\_3

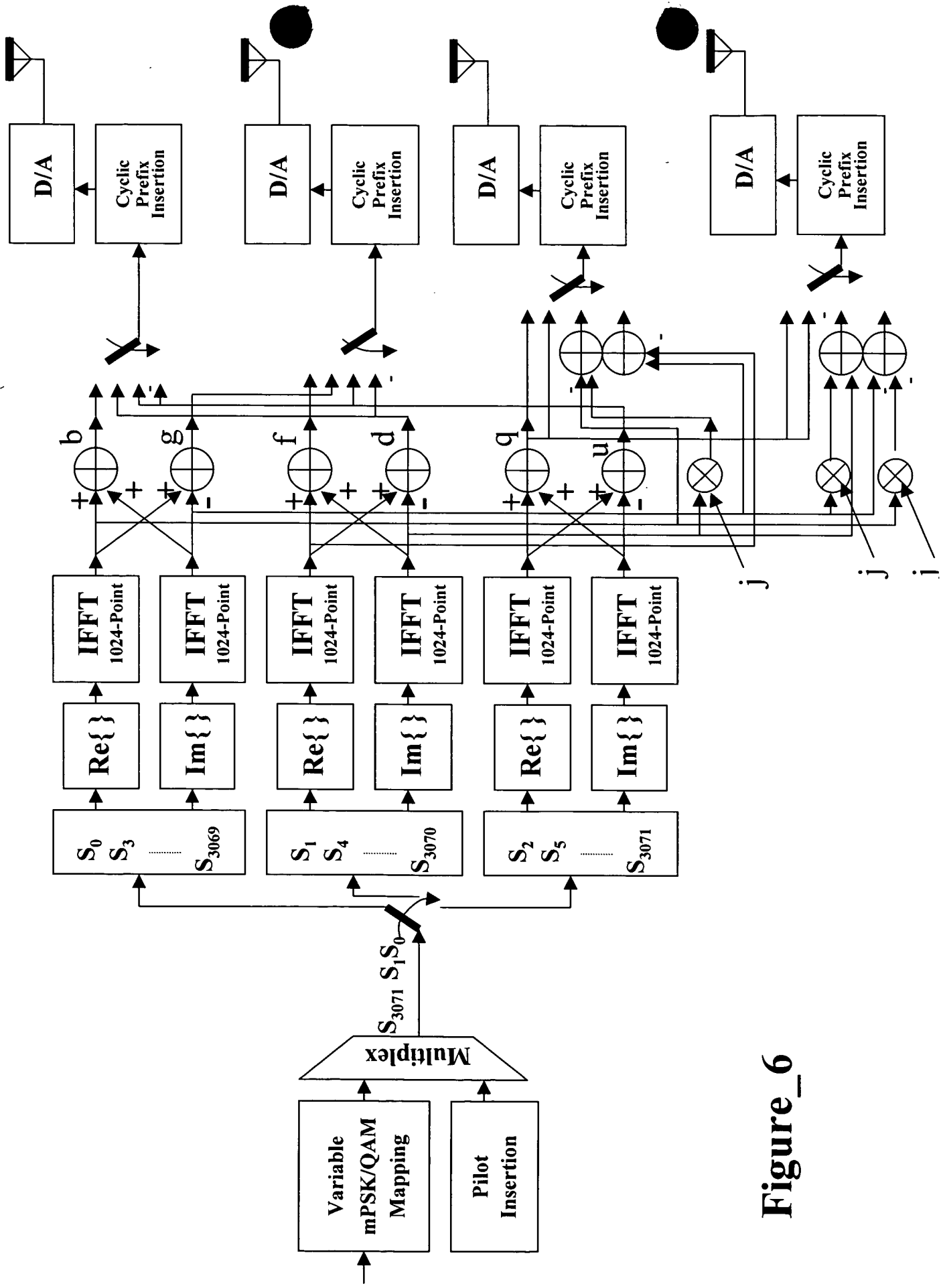


Figure\_4

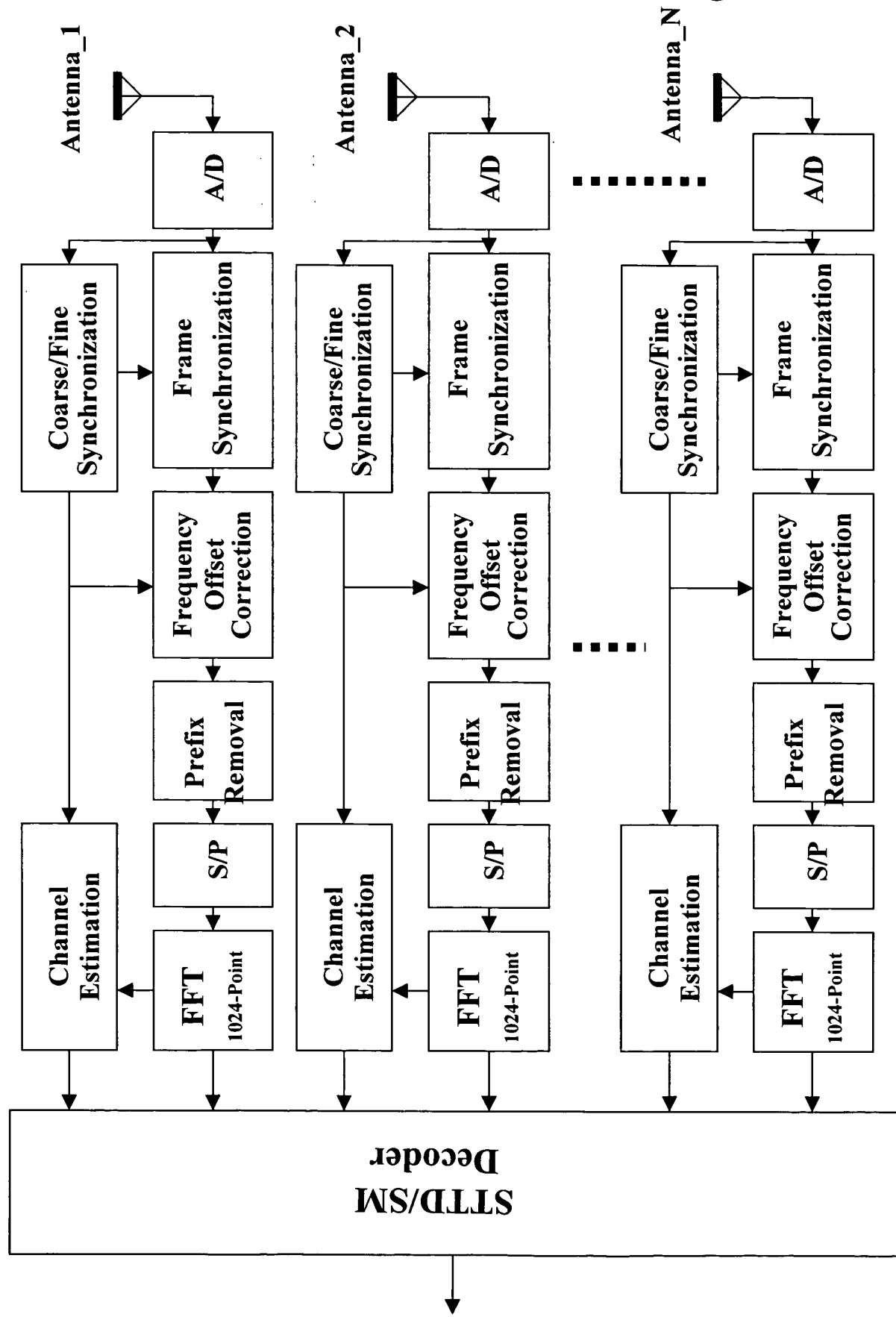


Figure\_5

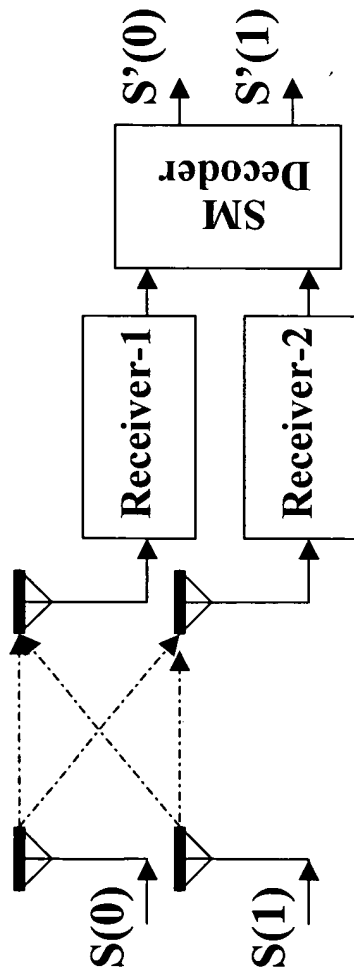
Figure 6 shows a block diagram of a multi-carrier communication system architecture. The system processes multiple data streams (S0, S1, S2, S3, S4, S5, ..., S3070, S3071) through a series of blocks including Variable mPSK/QAM Mapping, Pilot Insertion, Multiplexing, and IFFT processing. The outputs are then combined and sent to four separate D/A converters and antennas.



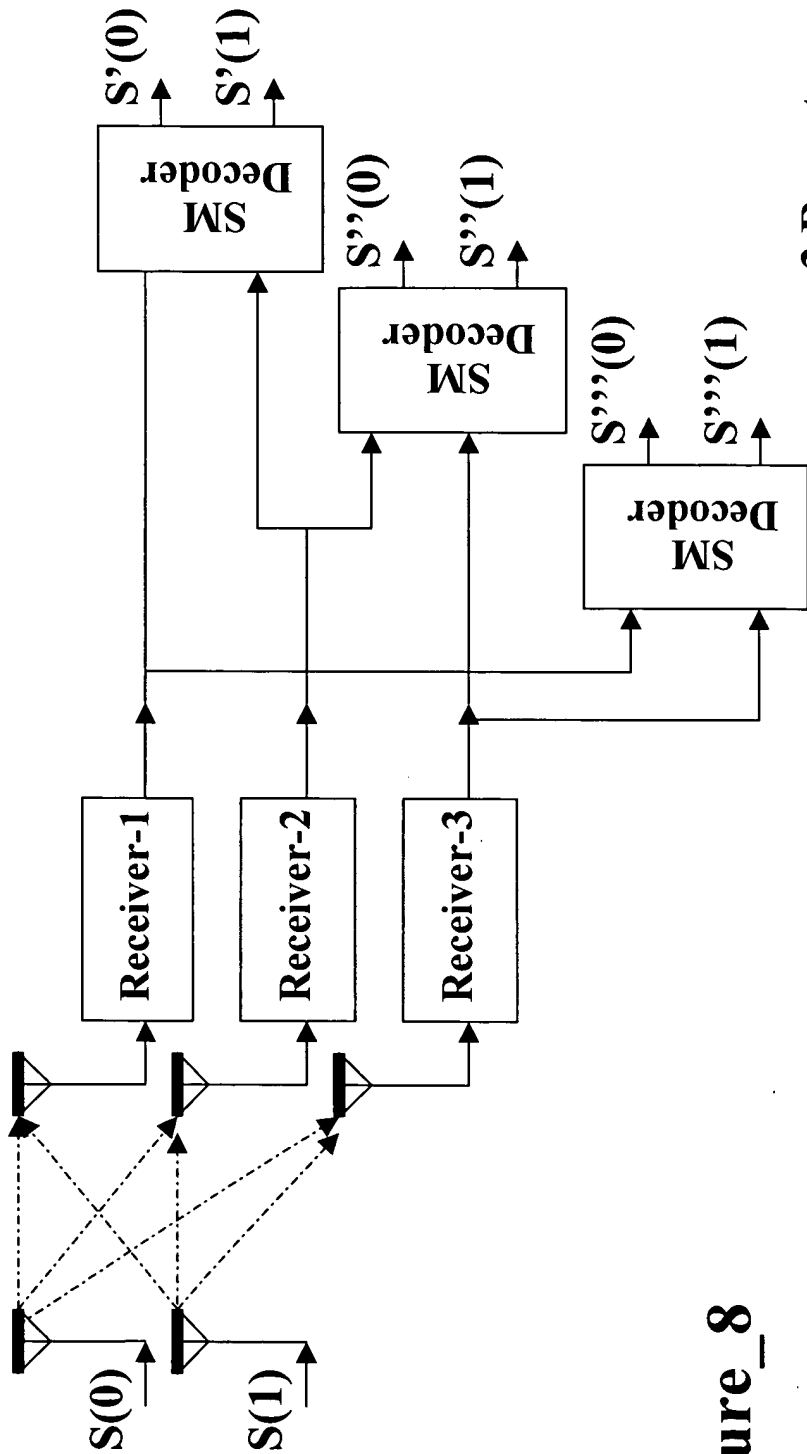
Figure\_6



**Figure\_7**



2 Rx antennas case



3 Rx antennas case

Figure\_8